UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/667,596	09/22/00	SONG I	2658-0190P

MM91/0726
BIRCH STEWART KOLASCH & BIRCH LLP
P O BOX 747
FALLS CHURCH VA 22040-0747

EXAMINER	
NGUYEN, H	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 07/26/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/667,596	SONG ET AL.	
	Examin r	Art Unit	
	HOAN C. NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-10,13,16-19,21-25 and 27-31* is/are rejected.

7)☒ Claim(s) *5,11,12,14,15, 20 and 26* is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2000* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the cited feature of "pixel electrode being connected to a source electrode" (claim 7) and "pixel electrode being connected to a drain electrode" (claim 9 or 10 or 13) on same a thin film transistor substrate must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the cited features of "the forming protective layer step forming the protective layer with a first contact hole exposing the source electrode part of metallic pattern" in claims 27-28 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The cited features in claims 7-10, 13, 27, 28 are not disclosed in specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 7-10, 13 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specification does not disclose how pixel electrode connected to both source electrode part and drain electrode part. Claims 7 and 9(or 10 or13) require both source and drain electrodes being connected to pixel electrode, this connection will short circuit of the source and drain electrodes, thus the data and gate lines could not drive the LCD. Besides, in conventional TFT substrate, if the drain electrode has connected to pixel electrode, the source electrode should be connected to data line for driving the liquid crystal cell.

5. Claims 27 and 28 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In specification, application does not show how to perform " a protective layer step forming the protective layer with a first contact hole exposing the source electrode part of the metallic pattern".

Claim Objections

6. Claims 11 and 14 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Both claims 11 and 14 depend on rejected claims 7 and 13 with further limit in that the pixel electrode is connected to both source and drain electrode parts of the metallic pattern.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 2, 6, 21, 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US5767926).

Kim discloses in Figs 11 and 12 that a thin film transistor substrate comprises (a) a plurality of gate lines 1 formed on substrate; (b) a plurality of data lines 5a insulated from and intersecting gate lines, date lines and intersecting gate lines defines a plurality of cells, at least one cell in including; (c) pixel electrode 4; (d) thin film transistor TFT on the gate line with source electrode connected to data line 5a; (e) metallic pattern 5b forming a drain electrode of the thin film transistor and storage electrode of capacitor (metallic layer above the first storage electrode 10 as disclosed in column 18, lines 11-15). The metallic pattern 5b is spaced a predetermined distance from the data line

connected to the thin film transistor; and a portion of a periphery of the pixel electrode overlaps metallic pattern as Figs. 11 and 20 shown. There is no protecting layer disposes between the pixel electrode and the metallic pattern. Kim also discloses in Fig. 16 that pixel electrode 4 overlaps a gate line 1. Kim further discloses in Fig. 7 the thin film transistor formed adjacent to each intersection of the gate lines and data lines.

2. Claims 23-25, 29-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin et al (US5737049).

Shin discloses in Figs 2A-F that the method of manufacturing a thin film transistor substrate comprises (a) forming a plurality date line with gate electrodes 21 extending therefrom on a transparent substrate; (b) forming gate insulating layer 24; (c) forming semiconductor layer 25/26 over at least a portion of one the gate electrodes, at least a portion of source electrodes and at least a portion of the drain electrodes; (d) forming a plurality data line intersecting with the gate line over the substrate, the data line including source electrode 29 extending therefrom (column 6, lines 57-65); (e) forming metallic pattern 30 having a drain electrode part and source electrode part, the source electrode part formed overlapping with one of gate lines, data lines and metallic pattern are formed simultaneously, and metallic layer is spaced predetermined distance from one of the data lines; (f) forming a protective film 31 over the substrate, the protective film including a contact hole 32-1 exposing a portion of the metallic pattern; (g) forming pixel electrode 33 over the protective film and in electrical contact with the metallic pattern via the contact hole.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3, 4,16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US5767926) in view of Bae (US5742363).

Kim discloses in Figs 11 and 12 that a thin film transistor substrate comprises (a) a plurality of gate lines 1 formed on substrate; (b) a plurality of data lines 5a insulated from and intersecting gate lines, date lines and intersecting gate lines defines a plurality of cells, at least one cell in including; (c) pixel electrode 4; (d) thin film transistor TFT on the gate line with source electrode connected to data line 5a; (e) metallic pattern 5b forming a drain electrode of the thin film transistor and storage electrode of capacitor (metallic layer above the first storage electrode 10 as disclosed in column 18, lines 11-15). The metallic pattern 5b is spaced a predetermined distance from the data line connected to the thin film transistor; and a portion of a periphery of the pixel electrode overlaps metallic pattern as Figs. 11 and 20 shown. There is no protecting layer disposes between the pixel electrode and the metallic pattern. Kim also discloses in Fig. 16 that pixel electrode 4 overlaps a gate line 1. Kim further discloses in Fig. 7 the thin film transistor formed adjacent to each intersection of the gate lines and data lines. However Kim does not disclose expressly that (a) protective layer disposes between the pixel electrode and the metallic pattern, the metallic pattern being overlapped with a portion of periphery of the pixel electrode; (b) pixel electrode is connected to drain electrode part of

the metallic pattern via a first contact hole in the protective layer; (c) protective layer includes a contact hole over a storage electrode part of metallic pattern.

Bae discloses in Figs. 4E-H that (a) protective layer disposes between the pixel electrode and the metallic pattern, the metallic pattern being overlapped with a portion of periphery of the pixel electrode; (b) pixel electrode is connected to drain electrode part of the metallic pattern via a first contact hole in the protective layer; (c) protective layer includes a contact hole over a storage electrode part of metallic pattern (column 3, lines 15-24).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a thin film transistor substrate as Kim disclosed. The modified thin film transistor substrate further comprises (a) protective layer disposes between the pixel electrode and the metallic pattern for forming contact hole and separating pixel electrode with source and drain electrodes (b) pixel electrode is connected to drain electrode part of the metallic pattern via a first contact hole in the protective layer for driving liquid crystal cell; (c) protective layer includes a contact hole over a storage electrode part of metallic pattern for forming storage capacitor to prevent voltage variation in the pixel electrode.

4. Claims 7, 8, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al (US5737049) in view of Morimoto (US6165810A).

Shin discloses in Figs 2A-F that the method of manufacturing a thin film transistor substrate comprises (a) forming a plurality date line with gate electrodes 21 extending therefrom on a transparent substrate; (b) forming gate insulating layer 24; (c)

forming semiconductor layer 25/26 over at least a portion of one the gate electrodes, at least a portion of source electrodes and at least a portion of the drain electrodes; (d) forming a plurality data line intersecting with the gate line over the substrate, the data line including source electrode 29 extending therefrom (column 6, lines 57-65); (e) forming metallic pattern 30 having a drain electrode part and source electrode part, the source electrode part formed overlapping with one of gate lines, data lines and metallic pattern are formed simultaneously, and metallic layer is spaced predetermined distance from one of the data lines; (f) forming a protective film 31 over the substrate, the protective film including a contact hole 32-1 exposing a portion of the metallic pattern; (g) forming pixel electrode 33 over the protective film and in electrical contact with the metallic pattern via the contact hole. However Shin fails to disclose a first contact hole exposing the source electrode part of metallic pattern.

Morimoto discloses in fig. 7 forming protective layer 42 with a first contact hole 43 exposing the source electrode part of metallic pattern 44.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the method of manufacturing a thin film transistor substrate as Shin disclosed. The modified method of manufacturing a thin film transistor substrate with forming protective layer with a first contact hole exposing the source electrode part of metallic pattern for providing another method of manufacturing the LCD.

Allowable Subject Matter

5. Claims 5, 12, 15, 20, 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: US5708483 to Asai and US5435324A to Brill.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (703)306-0472. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, SIKES L WILLIAM can be reached on (703)308-4842. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-5841 for regular communications and (703)308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0530.

HOAN C. NGUYEN
Examiner
Art Unit 2871

chn
July 5, 2001

William L. Sikes
William L. Sikes
Supervisory Patent Examiner
Technology Center 2800